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Series Compensation Technique for Grid voltage Synchronization for Distributed Generated System

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Abstract: **The use of series capacitors is to reduce the voltage drop in the lines with low power factor and improve the voltage at the receiving end particularly with low power factor loads. For variable load conditions, the voltage can be controlled by switching in suitable series capacitors in the line. Series compensation is defined as insertion of reactive power elements into transmission lines and provides the following benefits are reduce the voltage drops, increases the system response, stability and efficiency also increases the transfer capabilities. In order to achieve satisfactory results with such systems, it is necessary to count on accurate and fast grid voltage synchronization algorithms, which are able to work under unbalanced and distorted conditions. This project analyzes the synchronization capability of three advanced synchronization systems: the decoupled double synchronous reference frame phase-locked loop (PLL), the dual second order generalized integrator PLL, and the three-phase enhanced PLL, designed to work under such conditions. Although other systems based on frequency-locked loops have also been developed, PLLs have been chosen due to their link with dq0 controllers. The simulation results are presented by using Mat lab/Simulink software.**

Index Terms—Distributed Generated (DG) System, Grid Synchronization, Micro grid, series compensation controller.

I INTRODUCTION

A micro grid is a part of distribution network thatincludes multiple loads and distributed energy resourceconverters that are operated in parallel with the boarderutility grid [1]. It helps in integration of distributedenergy resource converters to micro grid. Micro grid is a partof distributed generation system. It is a localized groupingof electricity generation, energy storage and loads thatnormally operates connected to a traditional centralizedutility grid. The component of micro grid involvesdistributed generation resources such as photovoltaicpanels, small wind turbines, fuel cells, etc.

The storage devices are batteries, super capacitors,flywheel etc along with local loads. Better efficiency,superior quality with high reliability of power supplyhaving environmental as well as economical benefits can beachieved by using microgrid [2]. A droop control is a controltechnique applied to distributed generation system forprimary frequency control and as well as voltage controlfor load sharing between local loads to utility Grid.By controlling the frequency, as well as voltage,corresponding active power (P) and reactive power (Q) canbe controlled in distributed generation. Increase in activepower output results in reduction of frequency and thecorresponding increase in the reactive power results indecrease of voltage as explained in [3].

The concept of Phase Locked Loop (PLL) is used for theimplementation of grid synchronization method. PLL isused for the estimation of grid voltage, phase angle andfrequency. A PLL is a control system in which outputsignal is generated by relating its phase to the phase of aninput signal. A PLL can track an input frequency or it cangenerate a frequency that is a multiple of the inputfrequency as explained in [4]-[7].

This paper a series compensation controller based synchronization method is proposed for achieving the gridsynchronization in terms of frequency, phase angle,amplitude of output voltages, active power and reactivepower in between converter output and Distributed EnergyResource Converters (DERCs). The series compensation controlleris replaced by proportional integral (PI) controller forobtaining fast dynamic response, low steady error and for stable operation [8].

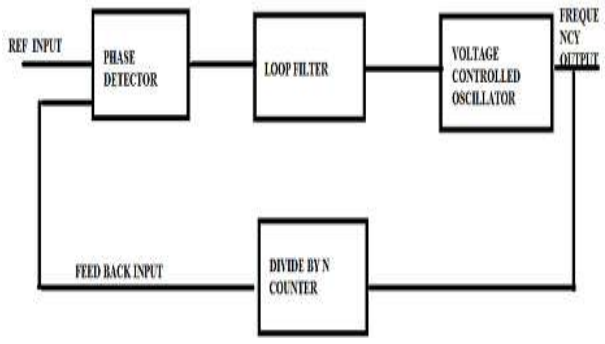

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Fig.1.Block Diagram of PLL Controller

The primary controller senses the difference voltagefrom the utility grid voltage and point of common couplingvoltage. A phase locked loop block is used in the primarycontroller to generate the input frequency signals from theprimary controller. A phase locked loop is a control loopwhich generates an output signal by comparing its phase tothe phase of an input signal. By maintaining the input and output frequencies lock step also implies keeping the inputand output frequencies the same. It can also sense afrequency, in addition of synchronizing the signals [9-10].

The concept on series compensation set theory was introduced by

L. A. Zadeh in 1965. Series compensation is rule based and it isapplication of human knowledge on system behavior as explained in. Fig.2 represents the schematicdiagram of series compensation based system.

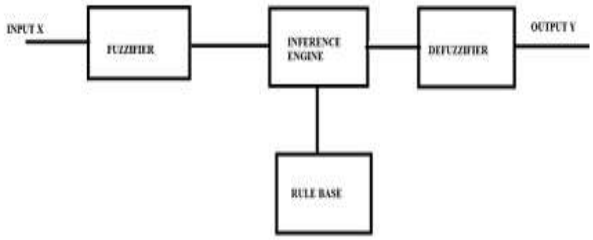

Fig 2: Schematic of Series compensation based system

Series compensation controller operation mainly involves the execution of four major operations:

- Fuzzification
- Rule based Inference system
- Composition and Defuzzification

Fuzzification involves the conversion of crisp values or classical set values toSeries compensation rule base values. It involves the choice of Variables, series compensation Input and output variables and the evaluation of membership functions. It involves series compensation subset rules, composition and defuzzification. For assigning each series compensation subset rule based value to the output variable a Rule based series compensation inference system is necessary. Composition helps in forming a Single series compensation subset rule based Value assigned to an output variable from a multiple rule based series compensation subset values. Defuzzification helps in the conversion of composition of series compensation rule based value to a single crisp value [11-12].

Defuzzification helps in the conversion of composition of series compensation rule based value to a single crisp value. A PI controller is replaced with a series compensation controller is as shown in fig.3.

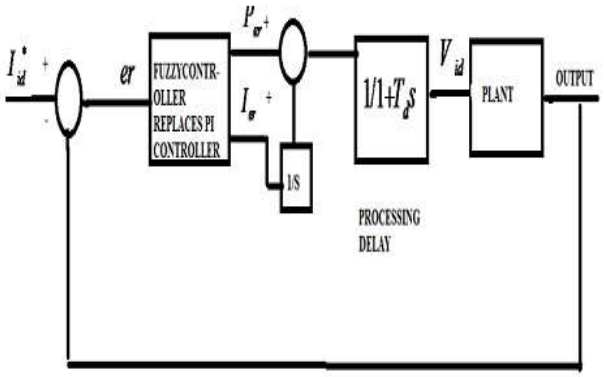

Fig 3: Block diagram of series compensation controller

The main objective of designing the Series compensation logic rules is to synchronize the grid parameters such as grid frequency, phase angle, amplitude of output voltages, active power and reactive power with the output of the distributed energy resource converters. The error and change of error are the inputs of the series compensation controller.

II GRID SYNCHRONIZATION ECIFICATIONS BASED ON GCR

Even though several works are published within the field ofgrid synchronization, almost all of them are centered on analyzing the individual dynamic performance of each proposal,without first determining a time response window within thedynamic behavior of the system under test, which would beconsidered to be satisfactory.In this paper, in order to evaluate the response of the gridsynchronization topologies under test, a common performancerequirement for all the structures has been established in thissection, considering the needs that can be derived from theLVRTrequirements.Despite the fact that the detection of the fault can be carriedout with simpler algorithms, as shown in and, theimportance of advanced grid synchronization systems lies in thenecessity of having accurate information about the magnitudeand phase of the grid voltage during the fault, in order to injectthe reactive power required by the TSO.In the German standard [2], it is stated that voltage controlmust take place within 20 ms after the fault recognition, byproviding a reactive current on the low voltage side of thegenerator transformer to at least 2% of the rated current for eachpercent of the voltage dip, as shown in Fig.4. 100% reactivepower delivery must be possible, if necessary.

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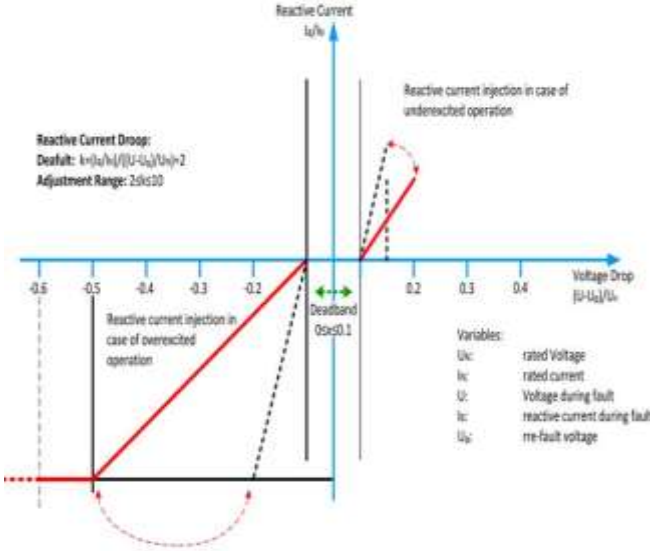

Fig.4. E-on voltage support requirement in the event of grid fault.

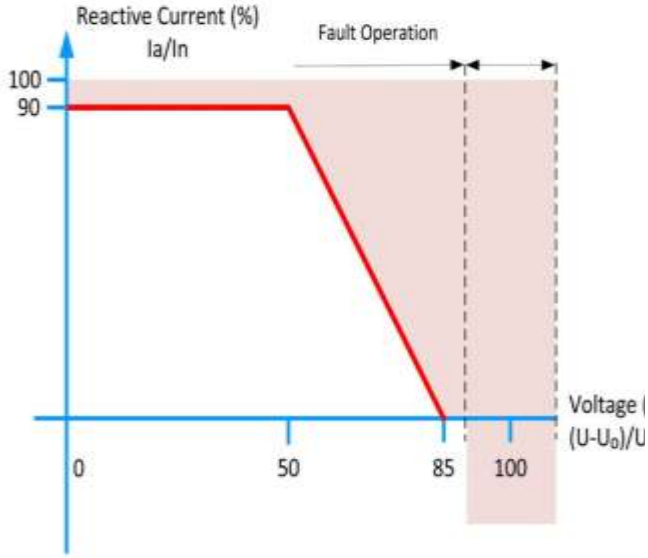

Fig.5. REE voltage support requirement in the event of grid fault.

A similar condition is given in the Spanish grid code, wherethe wind power plants are required to stop drawing inductivereactive power within 100 ms of a voltage drop and be able toinject full reactive power after 150 ms, as shown in Fig.5.

Considering these demands, this paper will consider that theestimation of the voltage conditions will be carried out within20–25 ms, as this target permits it to fulfill the most restrictiverequirements, in terms of dynamical response, available inthe grid codes. This condition will be extended to frequencyestimation; although this parameter is more related to secondarycontrol algorithms than LVRT, the same time window between20 and 25 ms will be considered in this work for the detectionof the disturbance.

III DESCRIPTION OF THE THREE SYNCHRONIZATION SYSTEMS

Many of the positive-sequence detection algorithms arebased on SRF PLLs. Despite having a good response underbalanced conditions, their performance becomes insufficient inunbalanced faulty grids (95% of cases), and their good operation is highly conditioned to the frequency stability, which isincompatible with the idea of a robust synchronization system.

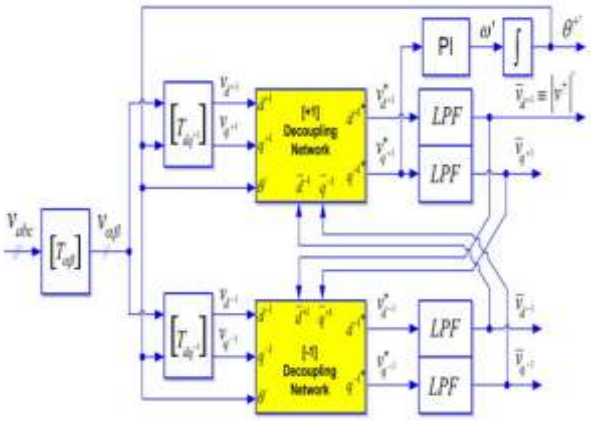

Fig.6. DDSRF-PLL block diagram.

Many authors have discussed different advanced models, whichare able to overcome the problems of the classical PLL, usingfrequency and amplitude adaptive structures which are able todeal with unbalanced, faulty, and harmonic-polluted grids. Inthe framework of these topologies, three PLL structures will bediscussed and evaluated in this paper.

A) DDSRF PLL

The DDSRF PLL published in and was developedfor improving the conventional SRF PLL. This synchronizationsystem exploits two synchronous reference frames rotating atthe fundamental utility frequency, one counterclockwise andanother one clockwise, in order to achieve an accurate detectionof the positive- and negative-sequence components of the gridvoltage vector when it is affected by unbalanced grid faults. Thediagram of the DDSRF PLL is shown in Fig.6.

When the three-phase grid voltage is unbalanced, the fundamental positive-sequence voltage vector appears as a dc voltageon the dq+1 axes of the positive-sequence SRF and as acvoltages at twice the fundamental utility frequency on the dq−1axes of the negative-sequence SRF. In contrast, the negativesequence voltage vector will cause a dc component on thenegative-sequence SRF and an ac oscillation on the positivesequence SRF. Since the amplitude of the oscillation on thepositive-sequence SRF matches the dc level on the negativesequence SRF and vice versa, a decoupling network is appliedto signals on the dq positive/negative SRF axes in order

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tocancel out such ac oscillations. Low-pass filters (LPFs) inFig.6 are responsible for extracting the dc component fromthe signal on the decoupled SRF axes. These dc componentscollect information about the amplitude and phase angle of thepositive- and negative-sequence components of the grid voltagevector.

Finally, the PI controller of the DDSRF PLL works on thedecoupled q-axis signal of the positive-sequence SRF (v∗q+1)and performs the same function as in an SRF PLL, aligning thepositive-sequence voltage with the d-axis. This signal is free ofac components due to the effect of the decoupling networks; thebandwidth of the loop controller can be consequently increased.

B) DSOGI PLL

The operating principle of the DSOGI PLL for estimatingthe positive- and negative-sequence components of the gridvoltage vectors is based on using the instantaneous symmetricalcomponent (ISC) method on the αβ stationary reference frame, as explained. The diagram of the DSOGI PLL is shownin Fig.7. As it can be noticed, the ISC method is implementedby the positive-sequence calculation block.

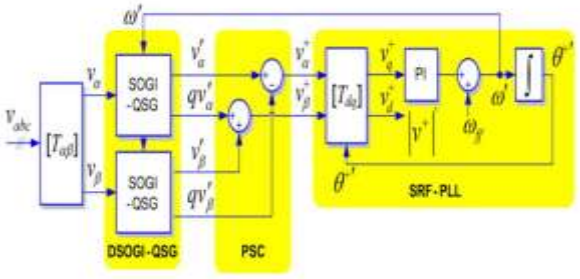

Fig.7. DSOGI-PLL block diagram.

To apply the ISC method, it is necessary to have a set ofsignals, $v\alpha$–$v\beta$, representing the input voltage vector on the $\alpha\beta$stationary reference frame together with another set of signals, $qv\alpha$–$qv\beta$, which are in quadrature and lagged with respectto $v\alpha$–$v\beta$. In the DSOGI PLL, the signals to be supplied tothe ISC method are obtained by using a dual second ordergeneralized integrator (DSOGI), which is an adaptive bandpass filter based on the generalized integrator concept.At its output, the DSOGI provides four signals, namely, $v\alpha$ and $v\beta$, which are filtered versions of $v\alpha$ and $v\beta$, respectively, and $qv\alpha$ *and*$qv\beta$, which are the in-quadrature versionsof $v\alpha$ and $v\beta$.

A conventional SRF PLL is applied on the estimatedpositive-sequence voltage vector, $v\alpha\beta$ +, to make this synchronization system frequency adaptive. In particular, the $v\alpha\beta$ + voltage vector is translated to the rotating SRF, and the signal onthe q-axis, v+q, is applied at the input of the loop controller.As a consequence, the fundamental grid frequency (ω) and the phase angle of the positive-sequence voltage vector (θ+) are estimated by this loop. The estimated frequency for thefundamental grid component is fed back to adapt the centerfrequency ω of the DSOGI.

C) 3phEPLL

The enhanced phase-locked loop (EPLL) is a synchronization system that has proven to provide good results in singlephase synchronization systems. An EPLL is essentiallyan adaptive bandpass filter, which is able to adjust the cut off frequency as a function of the input signal. Its structure waslater adapted for the three-phase case, in order to detectthe positive-sequence vector of three-phase signals, obtainingthe 3phEPLL that is represented in Fig.8.

In this case, each phase voltage is processed independentlyby an EPLL. This block filters the input signal and generatestwo sinusoidal outputs of the same amplitude and frequency,$vn$and j_{vn}, the second one being 90◦ with respect to vn.The resulting signals constitute the input for the computationalunit. Owing to these in-quadrature signals, the instantaneouspositive-sequence voltage component, v_{abc}+, can be estimatedby means of using the ISC method.

IV DISCRETE IMPLEMENTATION

The performance of the different structures under test is reallydependent on their final digital implementation, particularly onthe discretization approach made to their continuous equations.

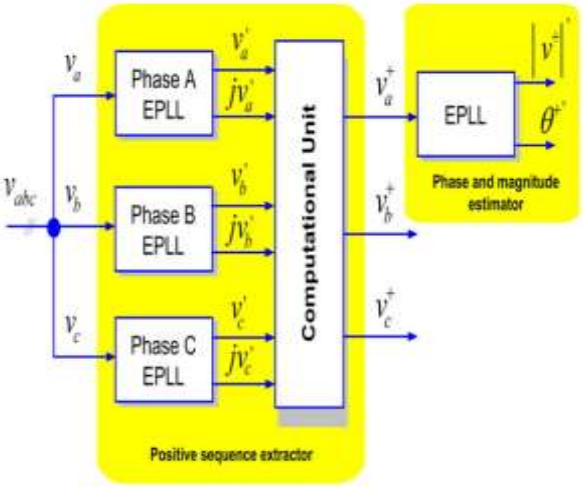

Fig.8. 3phEPLL block diagram.

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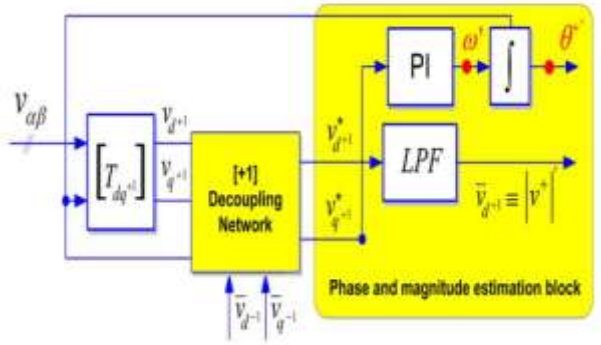

Fig.9.Phase and magnitude estimation loop of the DDSRF PLL.

This implementation is critical and should be studied indetail as a straightforward implementation can give rise to additional delays in the loop that hinder the good performance of thePLL. Some methods, such as the forward Euler, the backwardEuler, and the Tustin (trapezoidal) numerical integration, off area good performance when used for discrediting other synchronization systems. However, Eulermethods can be inadequate under certain conditions, due to theneed of introducing additional sample delays. Therefore,according to the specific needs of the presented topologies, thissection will describe the discrete representation of each PLLindividually. In order to facilitate the comprehension of theprocess, the different building blocks that appear at Figs. 6–8 will be referenced.

A) DDSRF-PLL Discretization

The discrete model of this PLL can be easily obtained sincethe continuous representation of several parts does not changein the discrete domain. This is the case for the transformationblocks Tαβ, Tdq+1, and Tdq−1, whose description can be found,in general, scope literature.

1) **Positive and Negative-Sequence Decoupling Networks:** The decoupling network constitutes one of the most important contributions of this synchronization method. The discrete equations of these blocks are shown in (1), being almost the same as in the continuous domain. It is just necessary to consider one sample delay of θ, $v\bar{}d-1$, $v\bar{}q-1$, $v\bar{}d+1$, and $v\bar{}q+1$ in order to avoid algebraic loops.

2) Phase and Magnitude Estimator Discretization: In the DDSRF PLL, the decoupling network appears embedded in the classical SRF-PLL loop (see Fig. 9). However, thisdoes not affect the discretization of the phase and magnitude estimator since v∗d+1 and vq∗+1 act as the input of this block

$$\begin{bmatrix} v^*_{d^+1}[n+1] \\ v^*_{q^+1}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d^+1}[n+1] \\ v_{q^+1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(2\theta'[n]) & -\sin(2\theta'[n]) \\ \sin(2\theta'[n]) & -\cos(2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d^-1}[n] \\ \bar{v}_{q^-1}[n] \end{bmatrix} \times \begin{bmatrix} v^*_{d^-1}[n+1] \\ v^*_{q^-1}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d^-1}[n+1] \\ v_{q^-1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(-2\theta'[n]) & -\sin(-2\theta'[n]) \\ \sin(-2\theta'[n]) & -\cos(-2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d^+1}[n] \\ \bar{v}_{q^+1}[n] \end{bmatrix} \quad (1)$$

The discrete controller and the integrator can be built using abackward numerical approximation. The frequency and phasecan then be represented in the z-domain (2), considering v∗q+1as the error to be minimized. In this equation, a feedforward ofthe nominal frequency is given by means of ωff.

$$W'(z) = \frac{(k_p + k_i \cdot T_s)z - k_p}{z-1} \cdot V^*_{q^+1}(z) + \omega_{ff}$$

$$\theta^{+'} = \frac{T_s \cdot z}{z-1} \cdot W'(z). \quad (2)$$

Finally, sample-based representation gives rise tohare the expressions to be implemented

$$\omega'[n+1] = \omega'[n] - k_p \cdot v^*_{q^+1}[n] + (k_p + k_i \cdot T_s) \cdot v^*_{q^+1}[n+1]$$

$$\theta^{+'}[n+1] = \theta^{+'}[n] + T_s \cdot \omega'[n+1] \quad (3)$$

In these equations, a frequency feedforward has been introduced as an initial condition to ω'.

3) **LPF Block Discretization:** The amplitudes of the dq positive- and negative-sequence components are the outputs of the decoupling networks. However, four infinite impulse responses (IIR) LPFs extract the ripple from each sequence estimation in order to reinforce the performance of the PLL in case of harmonic pollution. A first-order filter with a cutoff frequency ωf , equal to half of the grid frequency, was originally proposed in; hence, the same transfer function has been implemented in this paper for evaluation purposes in

$$y[n] = \frac{1}{T_s \cdot \omega_f + 1} \cdot x[n] + \frac{T_s \cdot \omega_f}{T_s \cdot \omega_f + 1} \cdot u[n]$$

$$x[n+1] = y[n]. \quad (4)$$

B) DSOGI-PLL Discretization

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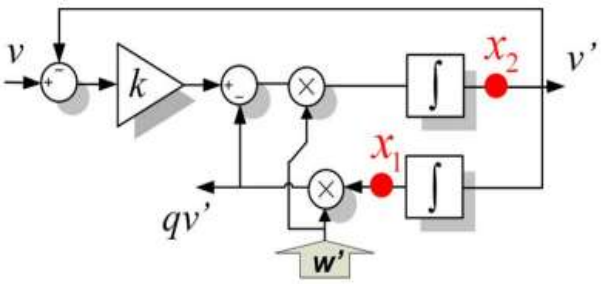
1) DSOGI-QSG Block Discretization: Aswas previously mentioned, the DSOGI-based quadrature signal generator (QSG) of Fig.10 consists of two independentand decoupled second-order generalized integrators (SOGIs).Therefore;each SOGI-based quadrature signal generator canbe discredited individually, thus facilitating it'sathematical description. In Fig.10, the block diagram of the implementedSOGI is shown.



SOGI - QSG

Fig.10. Quadrature signal generator based on a second order generalizedintegrator (SOGI QSG).

This quadrature signal generator (QSG) is a linear systemitself; therefore, a discrete representation can be systematicallyobtained if the continuous state space is previously deducted.The equations of the SOGI state space appear detailed in (5).where v constitutes the input while v and qv are the two inquadrature output signals

$$\left.\begin{aligned}\dot{x}_n &= A\cdot x_n + B\cdot v\\ y_n &= C\cdot x_n\end{aligned}\right\};\quad x_n=\begin{bmatrix}x_1\\x_2\end{bmatrix}\ y_n=\begin{bmatrix}v'\\qv'\end{bmatrix}$$
$$A=\begin{bmatrix}0 & 1\\ -\omega'^2 & -k\cdot\omega'\end{bmatrix}\ B=\begin{bmatrix}0\\k\cdot\omega'\end{bmatrix}\ C=\begin{bmatrix}0 & 1\\ \omega' & 0\end{bmatrix} \quad (5)$$

$$A'=\gamma\begin{bmatrix}1+2T_s\cdot k\cdot\omega'[n]-T_s^2\cdot\omega'^2[n] & 4T_s\\ -4T_s\cdot\omega'[n]^2 & 1-2T_s\cdot k\cdot\omega'[n]-T_s^2\cdot\omega'^2[n]\end{bmatrix},\ B'=\gamma\begin{bmatrix}2T_s\cdot k\cdot\omega'[n]\\ 4k\cdot\omega'[n]\end{bmatrix}$$
$$C'=\gamma\begin{bmatrix}-2T_s^2\cdot\omega'[n]^2 & 4T_s\\ 2T_s\cdot\omega'[n] & (2+T_s\cdot k\cdot\omega'[n])\end{bmatrix},\ D'=\gamma\begin{bmatrix}2T_s\cdot k\cdot\omega'[n]\\ k\cdot T_s^2\cdot\omega'[n]^2\end{bmatrix}$$
$$\gamma=\frac{1}{4+2\cdot T_s\cdot k\cdot\omega'[n]+T_s^2\cdot\omega'^2[n]} \quad (6)$$

The discretization of this system has been performed usingtrapezoidal integrators, as they offer a better detection of thephase, which is important when dealing with sinusoidal signal. The symbolic values of each matrix of (7) are detailed in (6), shown at the bottom of the page. In these matrices, Ts isthe sampling time of the discrete system, ω'[n] is the estimatedfrequency magnitude, which comes from the estimation madeat the SRF-PLL block at each computation step, and k is theSOGI gain

$$\begin{aligned}x[n+1] &= A'\cdot x[n] + B'\cdot v[n]\\ y[n] &= C'\cdot x[n] + D'\cdot v[n].\end{aligned} \quad (7)$$

The discrete state space of (6) is obtained from the continuous representation by means of the mathematical procedure

$$A'=\left(I+\frac{A\cdot T_s}{2}\right)\left(I-\frac{A\cdot T_s}{2}\right)^{-1}$$
$$B'=\left(I-\frac{A\cdot T_s}{2}\right)^{-1}\cdot B$$
$$C'=T_s\cdot C\cdot\left(I-\frac{A\cdot T_s}{2}\right)^{-1}$$
$$D'=C\cdot\left(I-\frac{A\cdot T_s}{2}\right)^{-1}\cdot\frac{B\cdot T_s}{2} \quad (8)$$

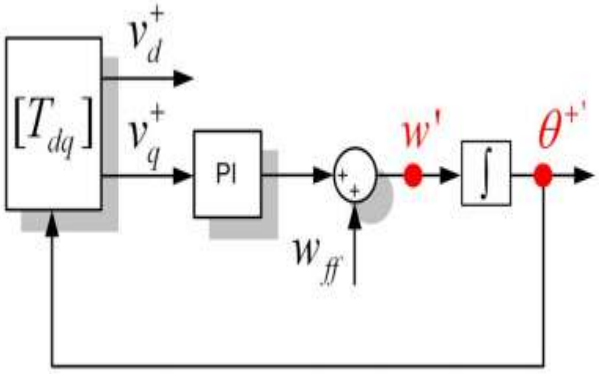


Fig.11. State variables of the SRF-PLL block.

WhereTs is the sampling time.The resulting discrete system is the best option as it reducesthe need of using additional delays for breaking algebraic loopsthat appear using other methods which do not consider theSOGI QSG as a whole.

2) SRF PLL Discretization: The frequency and phase detection is obtained by means of the SRF PLL shown in Fig.11. Thediscretization of the controller and the integrator is performedusing the backward numerical approximation.The frequency and phase can then be represented in thez-domain, as shown in (9), where v+q constitutes the error tobe minimized

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$$W'(z)=\frac{(k_p+k_i\cdot T_s)z-k_p}{z-1}\cdot V^*_{q+1}(z)+\omega_{ff}$$

$$\theta^{+'}=\frac{T_s\cdot z}{z-1}\cdot W'(z).$$

(9)

It can be noticed that the previous equations in (9) are equalto (2), as, in both cases, an SRF PLL is implemented. Likewise, the sample-based representation of (9) can be written asshown in

$$\omega'[n+1]=\omega'[n]-k_p\cdot v^*_{q+1}[n]+(k_p+k_i\cdot T_s)\cdot v^*_{q+1}[n+1]$$

$$\theta^{+'}[n+1]=\theta^{+'}[n]+T_s\cdot\omega'[n+1]$$

(10)

This three-phase grid synchronization system exploits theEPLL as a quadrature signal generator. An independent EPLLis used for processing each one of the three-phase voltages. Thesame EPLL structure is applied again to detect the magnitudeand phase of the positive-sequence voltage component.

1) QSG Block—EPLL Discretization: The block diagram of the EPLL implemented in this paper is presented in Fig.12.

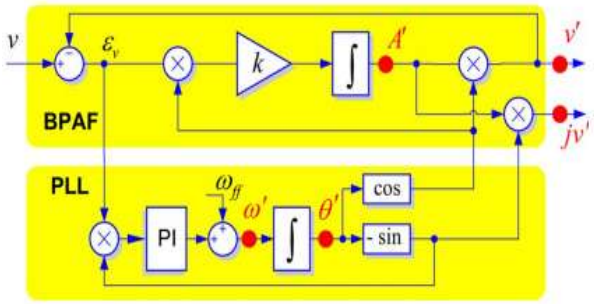

Fig.12. Quadrature signal generator based on an EPLL structure

According to this diagram, the state space representation ofthe EPLL in the continuous domain can be written as shown in

$$\dot{A}'(t)=k\cdot e(t)\cdot\cos\theta'(t)$$

$$\dot{\omega}'(t)=-k_i\cdot e(t)\cdot\sin\theta'(t)$$

$$\dot{\theta}(t)=\omega'(t)+\frac{k_p}{k_i}\cdot\dot{\omega}'(t).$$

(11)

The discrete state space variable representation using a forward Euler approximation to rechastisefactory results; therefore, the same method has been implemented here

$$e[n+1]=u[n+1]-v'[n]$$

$$A'[n+1]=A'[n]+T_s\cdot k\cdot e[n]\cdot\cos(\theta'[n])$$

$$\omega'[n+1]=\omega'[n]-T_s\cdot k_i\cdot e[n]\cdot\sin(\theta'[n])$$

$$\theta'[n+1]=\theta'[n]+T_s\cdot\omega'[n]-T_s\cdot k_p\cdot e[n]\cdot\sin(\theta'[n])$$

(12)

Finally, after the state variables are calculated, the EPLL output can be obtained by (13), generating the two quadraturesignals

$$v'[n+1]=A'[n+1]\cdot\cos(\theta'[n+1])$$

$$qv'[n+1]=-A'[n+1]\cdot\sin(\theta'[n+1]).$$

(13)

This type of discretization method needs a more accuratetuning, due to the fact that the stable regions of the s-planeand z-plane are different. However, its major simplicity,compared to the Tustin or backward integration, benefits fromthe computational speed of this block.

2) Computational Block Unit: The description for this blockis the same in both discrete and continuous domains. Nevertheless, specific equations are used in this paper, as shown in (14).

3) Phase and Magnitude Detection Block: This element isbased on another EPLL, which is responsible for estimating the phase and the magnitude of the Positive-sequence fundamentalcomponent.Its discretization is equal to that shown in (12).

$$v^+_a[n]=\frac{1}{3}v'_a[n]-\frac{1}{6}(v'_b[n]+v'_c[n])+\frac{1}{2\sqrt{3}}(jv'[n]_b-jv'_c[n])$$

$$v^+_c[n]=\frac{1}{3}v'[n]_c-\frac{1}{6}(v'_a[n]-v'_b[n])+\frac{1}{2\sqrt{3}}(jv'_a[n]-jv'_b[n])$$

$$v^+_b[n]=-(v^+_a[n]+v^+_c[n])$$

(14)

V SERIES COMPENSATION

Series Compensation Method A dynamic voltage restorer (DVR) was introduced for mitigating a voltage sag. The DVR is based on an Voltage source converter (VSC) system that has energy storage for supplying active power, an output filter to make output voltage wave sinusoidal, and a step up transformer connected in series with line.

A DVR is configured as a series-connected voltage controller. To control the output voltage of the DVR, the inverter supplies the missing load voltage using self-commutable electronic switches such as a gate turn-off thyristor (GTO), or an insulated gate bipolar transistor (IGBT), or an insulated gate commutated thyristor

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(IGCT). A DVR injects the missing voltage in series; it can be called a series voltage controller, but the term DVR is commonly used now. The advantages of the DVR are fast response, ability to compensate for voltage sag and a voltage phase shift using an inverter system. Three schemes can be used to generate the missing voltage in series with the source voltage for compensating the voltage sag such as,

In-phase voltage injection

- Phase-invariant voltage injection
- Phase advanced voltage injection
- In the in-phase voltage injection scheme,

The injecting voltage has the same phase angle of the source voltage. Therefore, the magnitude of the injected voltage is the smallest among three compensation schemes. However, this scheme requires the largest active power. In case of the phase invariant voltage injection scheme, the DVR injects the missing voltage that keeps the magnitude of the voltage as well as the phase of the supply voltage. This scheme needs a large injected voltage and may cause over injection of reactive power. Since the size of energy storage is closely related to the requirement of active power, various compensation methods to reduce the requirement of active energy have been proposed. If the injected voltage is in quadrature with the load current, the DVR does not inject active power. This scheme is highly dependent on the load power factor and may generate a sudden jump of the voltage phase angle. To avoid sudden phase angle jump, the phase of the injected voltage should be gradually changed at the beginning of the compensation as well as at the restoration in order not to disturb the operation of sensitive loads. The high-speed PWM switching and output filter makes it possible to achieve a fast response with less harmonic distortion. However, DVR are expensive because of the converter systems, the inserting transformer, and energy storages to supply active and reactive power for the missing voltage.

VI MATLAB/SIMULATION RESULTS

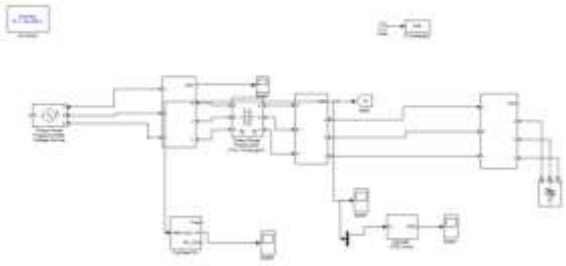

Fig 13 Matlab/simulation circuit of decoupled double synchronous reference frame PLL (DDSRF PLL)

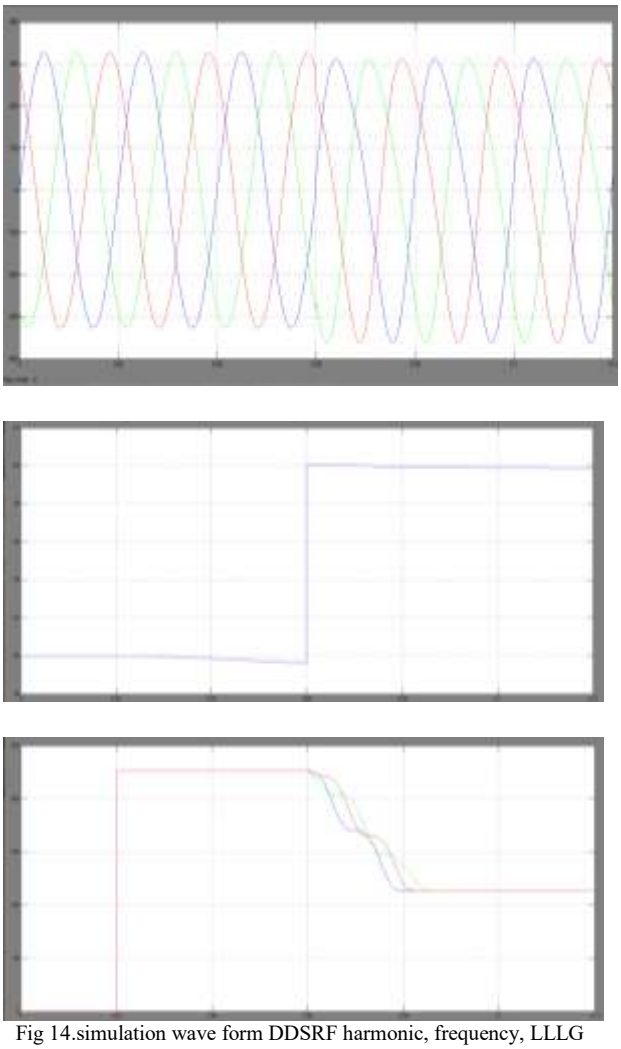

Fig 14.simulation wave form DDSRF harmonic, frequency, LLLG and unbalance condition

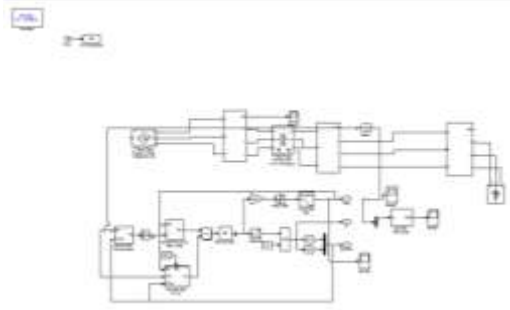

Fig 15 Matlab/simulation circuit of dual second order generalized integrator PLL

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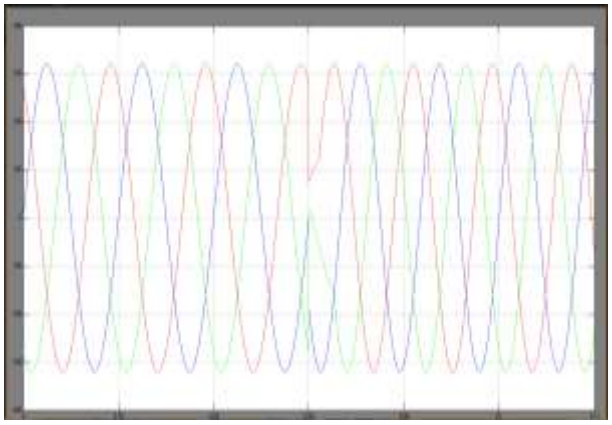
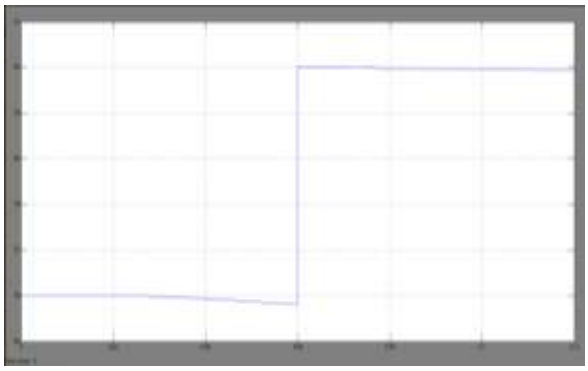
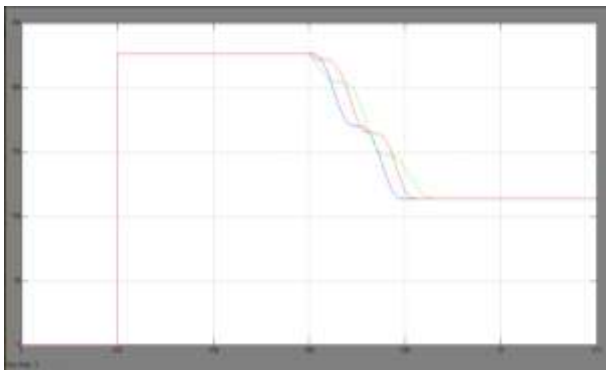






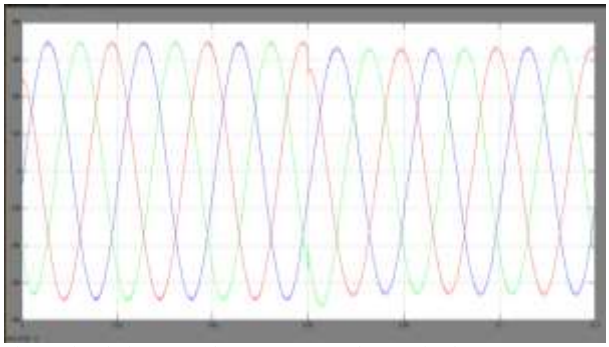


Fig.16 simulation wave form DSOGPLL harmonic, frequency, LLLG and unbalance condition

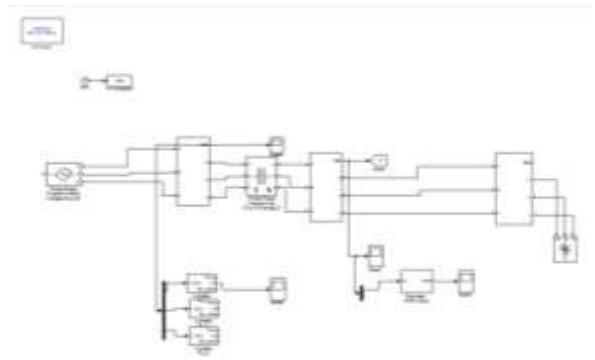
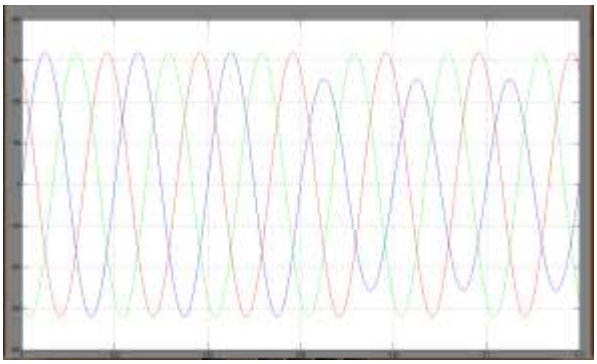
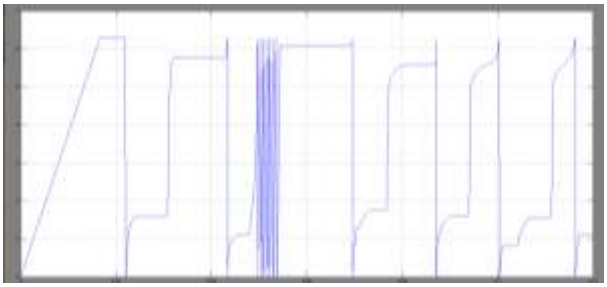
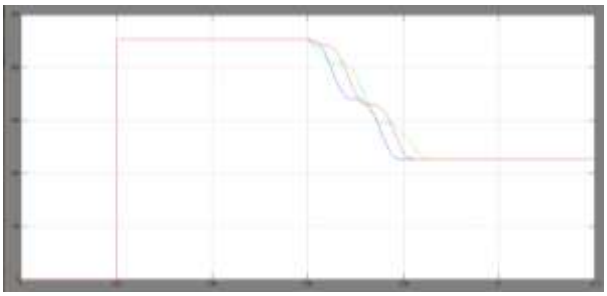


Fig 17 Matlab/simulation circuit of three-phase enhanced PLL (3phEPLL)







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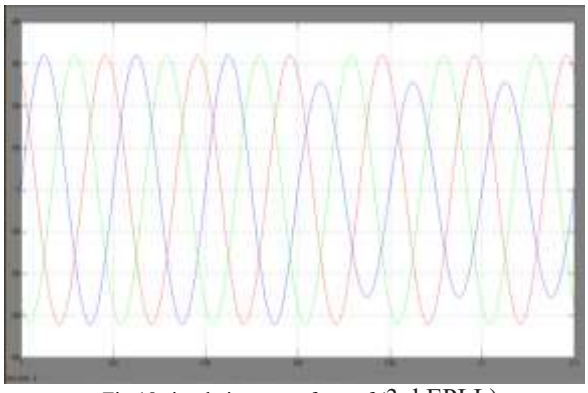


Fig 18 simulation wave form of (3phEPLL)
Harmonic, frequency, LLLG and unbalance condition

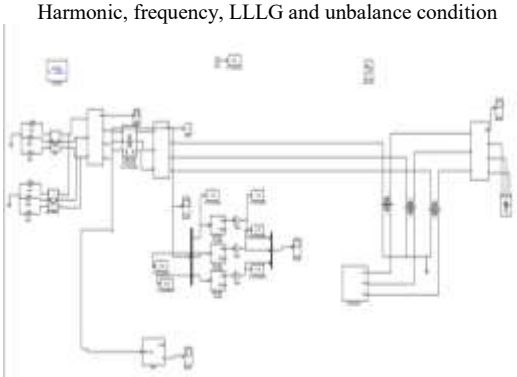
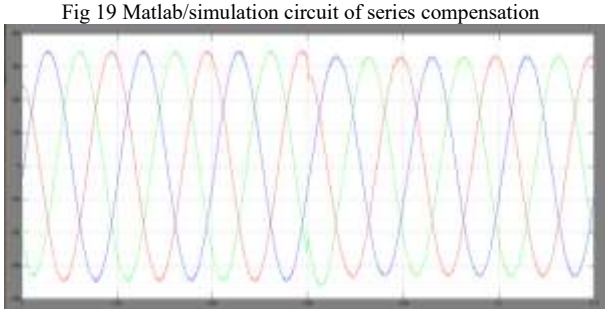
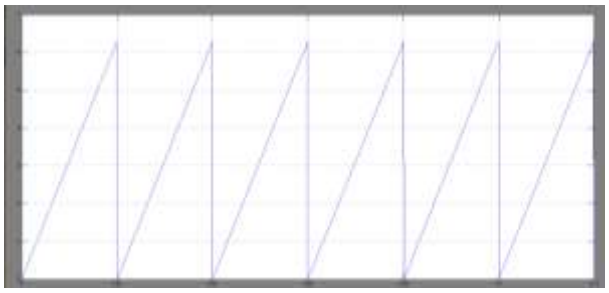


Fig 19 Matlab/simulation circuit of series compensation





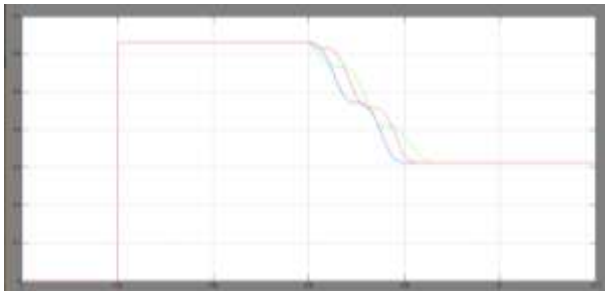


Fig 20 simulation wave form of series compensation
Harmonic, frequency, LLLG and unbalance condition

VI CONCLUSION

This paper developed a Series compensation based Grid voltage Synchronization for Distributed Generated System. A series compensation based secondary controller is used for achieving the grid synchronization by integrating the distributed energy resource converters to micro grid. The simulation results with series compensation controller helps in obtaining the quick response, low steady state error and reduces the harmonics with low ripple content. The power factor is also improved near PCC and power quality has been increased by the influence of multiple types of DG sources in distribution generation system. Hence, the proposed series compensation system has better performance for achieving grid synchronization. The DDSRF PLL and the DSOGI PLL allow estimating the ISCs of a three-phase system working in the αβ reference frame, while the 3phEPLL uses the "abc" reference frame, thus working with three variables. As has been shown, this feature simplifies the structure of the DSOGI PLL and the DDSRF PLL, which allows reducing the computational burden, as compared to the 3phEPLL, without affecting its performance.

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